

**REMARKS/ARGUMENTS**

Claims 1-20 remain pending in the subject application. Claims 1, 5, 8, 9, 14, 19 and 20 have been amended, as recited hereinabove.

Claims 1, 9 and 14 have been objected thereto on the basis of certain informalities, which are now rendered moot in light of amendments to claims 1, 9 and 14.

Claims 1 – 7 and 9-20 have been rejected, under 35 U.S.C. 102(e) as allegedly being anticipated by Grieff et al. (US Patent 6,961,813) (hereinafter “Grieff”) in view of Talati (US Patent No. 6,763,402) (hereinafter “Talati”). It appears that this rejection should have been under 35 U.S.C. 103(a) rather than 102(e), correction is therefore respectfully requested to this rejection in subsequent correspondences. It is believed that independent claims 1, 9, 14 and 19 and all claims depending therefrom are patentable over Grieff in view of Talatifer, inter alia, the following reasons.

In the claimed invention, the first and second task files are each separately responsive to non-data FIS from the first and second host units, respectively, and as such they allow for “concurrently accessing the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, ...”. Furthermore, arbitration is not performed until after non-data FIS have been stored in the task files. In contrast thereto, Talati uses a single queue, i.e. buffer RAM 194 and performs arbitration of commands prior to queuing, which are some of the reasons, among others, for preventing Talati from “accepting commands, from either host, at any given time”. [See Talati: Col. 5, lns. 26-30].

Moreover, the combination of Grieff and Talati is believed to be erroneous as Talati is directed to the problem of interfacing a data storage device, a SATA device, to a plurality of host data processing systems, through an IEEE 1349a bus and therefore uses bridges to convert the interface protocols and, whereas, Grieff is directed to a switch receiving input, through SATA ports, from multiple host devices and an arbiter module for assigning a priority scheme to received commands and for transmission thereof to a storage device through SATA ports. Therefore, Talati would not have been motivated to solve the problem solved by the claimed invention by using the teachings of Grieff, as Talati did not consider receiving input from SATA ports.

Thus, it is believed that claims 1, 9, 14 and 19 are patentable over Grieff in view of Talati and therefore, all claims depending therefrom are necessarily patentable over Grieff


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in view of Talati. It is further believed that for the foregoing reasons, claim 8 is patentable over Grieff in view of Talati and further in view of Kreifels (US Patent No. 4,891,788).

Reconsideration and allowance of claims 1-20 is hereby respectfully requested. Applicants submit that the subject application is now in condition for allowance and an early notice thereof is respectfully requested. Should any further amendment be required prior to passing the application to issue, the Examiner is respectfully invited to contact the undersigned by telephone at the number set out below.

Respectfully submitted,  
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I hereby certify that this correspondence with all attachments is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450 on November 6, 2006 by Erika Villafana.

